What Is Claimed Is:

1. An electrostatic discharge (ESD) protection circuit with low input capacitance, suitable for an I/O pad, comprising a plurality of diodes, stacked and coupled between a first power line and the I/O pad, wherein during normal operation, the diodes are reverse-biased, and, when an ESD event occurs between a second power line and the I/O pad, the diodes are forward-biased to conduct ESD current.

2. The ESD protection circuit as claimed in claim 1, wherein each diode is a PN junction diode formed by placing a doped area of a first conductivity type in a first well of a second conductivity type, a deep well of the first conductivity type formed under the first well to isolate the first well from a substrate of the second conductivity type.

3. The ESD protection circuit as claimed in claim 2, wherein the first well is surrounded by a second well of the first conductivity type.

4. The ESD protection circuit as claimed in claim 2, wherein the first conductivity type is N type, and the second conductivity type is P type.

5. The ESD protection circuit as claimed in claim 1, wherein the ESD protection circuit further includes a power-rail ESD clamp circuit, set between a first power line and a second power line, the power-rail ESD clamp circuit being turned on to conduct ESD current when an ESD event occurs.

6. The ESD protection circuit as claimed in claim 5, wherein the power-rail ESD clamp circuit includes a substrate-triggered MOS of the first conductivity type, the substrate-triggered MOS including two source/drains and a substrate, the two source/drains coupled to the first power line and the second power line respectively, the substrate node biased with suitable current to trigger a bipolar junction transistor parasitizing in the substrate-triggered MOS, and conducting ESD current when an ESD event occurs.

7. The ESD protection circuit as claimed in claim 6, wherein the substrate-triggered MOS includes a gate applied with a first bias voltage to keep the substrate-triggered MOS off during normal operations.

8. The ESD protection circuit as claimed in claim 6, wherein the gate is applied with a second bias voltage to speed up the turn-on rate of the substrate-triggered MOS when an ESD event occurs.

9. The ESD protection circuit as claimed in claim 6, wherein the substrate-triggered MOS is formed in a first well of a second conductivity type, a deep well of a first conductivity type being formed under the first well to isolate the first well from a substrate of the second conductivity type.

10. The ESD protection circuit as claimed in claim 9, wherein the first well is surrounded by a second well of the first conductivity type.

11. The ESD protection circuit as claimed in claim 5, wherein the power-rail ESD clamp circuit includes an ESD detection circuit to detect the occurrence of the ESD event.

12. The ESD protection circuit as claimed in claim 1, wherein one of the diodes is a MOS diode with a gate coupled to a source/drain of the MOS diode.

13. The ESD protection circuit as claimed in claim 1, wherein the diode includes a PN junction diode formed by a PN junction between a source/drain and a substrate of a MOS.

14. The ESD protection circuit as claimed in claim 13, wherein the gate of said MOS is coupled to the first power line.

15. The ESD protection circuit as claimed in claim 13, wherein the gate of said MOS is coupled to another source/drain of the MOS.

16. The ESD protection circuit as claimed in claim 13, wherein the MOS is PMOS.

17. The ESD protection circuit as claimed in claim 13, wherein the MOS is NMOS.

18. A power-rail ESD clamp circuit, suitable for an integrated circuit, coupled between two power lines, comprising:
a substrate-triggered MOS, including:
a gate;

two source/drains, respectively coupled to two power lines; and

a substrate; and

an ESD detection circuit, providing a bias current to the substrate of the MOS, and a bias voltage to the gate of the MOS element to trigger the MOS and conduct ESD current when an ESD event occurs.

19. The power-rail ESD clamp circuit as claimed in claim 18, wherein the power-rail ESD clamp circuit further comprises a voltage clamp circuit coupled between the gate and one of the two power lines to limit the bias voltage.

20. The power-rail ESD clamp circuit as claimed in claim 19, wherein the voltage clamp circuit is formed by one diode forward-biased when the ESD event occurs.

21. The power-rail ESD clamp circuit as claimed in claim 19, wherein the voltage clamp circuit is formed by a plurality of stacked diodes forward-biased when the ESD event occurs.

22. The power-rail ESD clamp circuit as claimed in claim 19, wherein the voltage clamp circuit is formed by a Zener diode reverse-biased to clamp the bias voltage at a breakdown voltage when ESD event occurs.

23. The power-rail ESD clamp circuit as claimed in claim 18, wherein one of the two power lines is a high voltage power line, the other is a low voltage power line, and the substrate-triggered MOS is an NMOS.

24. The power-rail ESD clamp circuit as claimed in claim 18, wherein said ESD detection circuit comprising:
an RC-based circuit for detecting the ESD event; and
a driver controlled by the RC-based circuit, for driving the gate and the substrate of the substrate-triggered MOS.

25. The power-rail ESD clamp circuit as claimed in claim 24, wherein the RC-based circuit includes a resistor and a capacitor, connected in series between the two power lines.

26. The ESD clamp circuit between power lines as claimed in claim 24, wherein the driver includes an inverter, having an output node coupled to the gate and the substrate of the substrate-triggered MOS.